ABSTRACT

A data recovery system for a serial digital data link includes a data sampler, compare logic, a phase controller, and a phase shifter. The data sampler samples input data three times in a bit time which time is determined by clock pulses generated by the phase shifter, and recovers digital data according to a predetermined decision criterion. Data sampling phases are split so as to track the data eye. The compare logic compares the output of the data sampler according to a predetermined method. Phase controller uses the output of the compare logic and generates phase control signals. These signals are set so as to control the sampling times of the data sampler and to attain near optimally recovered data stream. The phase shifter uses the phase control signals and makes three different phase clocks from input clock. The input clock can be an external clock, or can be recovered from the external clock or input data stream.